THE MODULAR DESIGN OF LUMPED PARAMETER DELAY NETWORKS

John James Downing

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THE MODULAR DESIGN OF LUMPED PARAMETER DELAY NETWORKS

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John J. Downing

THE MODULAR DESIGN OF LUMPED PARAMETER DELAY NETWORKS

by

John James Downing

Submitted in partial fulfillment
of the requirements
for the degree of
MASTER OF SCIENCE
IN
ENGINEERING ELECTRONICS

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Thesis
D705

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the thesis requirements for the degree of

MASTER OF SCIENCE

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PREFACE

Concerned about the increasing complexity of electronic equipment and the time required to manufacture it, the Navy Bureau of Aeronautics, in 1950, requested the National Bureau of Standards to attempt to devise a mechanized production system. Two years ago this agency succeeded in designing a pilot plant, bearing the name Project Tinkertoy, which is perhaps the closest approach to an automatic factory outside of the printing industry.

The Modular Design and Mechanized Production of Electronics, as it is now called, is stimulating an ever increasing interest on the part of a mass production conscious radio industry in the United States. The work herein reported was conducted under the sponsorship of American Car and Foundry Electronics, currently the foremost commercial promoter of Modular Design for Electronics (MDE).

It is the purpose of this paper to demonstrate the evolution of a modularized circuit, with particular emphasis on the problems encountered in achieving compatibility of electrical requirements with the mechanical constraints imposed by the module. The case herein treated is especially critical in this respect.

The author wishes to thank Professor Robert L. Miller of the U. S. Naval Postgraduate School for his assistance in securing the project, and for his cooperation in obtaining experimental results and in the preparation of this paper.

TABLE OF CONTENTS

Item	Title	Page
Chapter I	Introduction	1
Chapter II	Delay Line Theory	4
Chapter III	Inductance Considerations	12
Chapter IV	Modular Configuration	21
Chapter V	Terminations	27
Chapter VI	Design Aids	30
Chapter VII	Experimental Construction and Results	37
Chapter VIII	Conclusion	46
Bibliography		50
Appendix I	Rise Time of Multi-section Delay Network	51
Appendix II	Delay Line Design Equations	54
Appendix III	Multilayer Coil Design	58

LIST OF ILLUSTRATIONS

Figure		Page
1.	Transmission and Phase Behavior of a Low Pass Filter	5
2.	Development of m-derived Delay Line Section	13
3.	Normalized Self Inductance vs. Inside Diameter for Multilayer Coils	16
4.	Coupling Coefficient vs. Radial Thickness for Multilayer Coils	17
5.	Radial Thickness vs. Inside Diameter for Coupling Coefficient Between Multilayer Coils = 0.24 to 0.28	19
6.	Modular Arrangements for Inductors	22
7.	Line Configurations and Terminations	24
8.	Delay Line Design Nomograph No. 1	32
9.	Delay Line Design Nomograph No. 2	33
10.	Delay Line Design Nomograph No. 3	34
11.	Modular Layout for Delay Line	40
12.	Delay Line Test Setup	42
13.	Illustration of Appendix I Manipulations	52
14.	Illustration of Appendix III Procedure	58

CHAPTER I

INTRODUCTION

1. The Module

The first step in the development of MDE consisted of a review of known techniques and materials which would be adaptable to mechanization. The results of this study, undertaken at the National Bureau of Standards, indicated that the most compatible techniques would be to employ printed circuits, miniaturized parts, and to substitute wherever practicable, specially fabricated components for the conventional resistors and capacitors normally used in electronic subassemblies.

Tape resistors, a National Bureau of Standards development, appeared to constitute a likely substitute for conventional resistors; extensive use of high dielectric constant ceramic capacitors afforded the solution to the capacitor problem. These components were to be mounted on ceramic wafers that could then be stacked skyscraper fashion to form a module. Interconnection between the components as well as mechanical support for the wafer stack is provided by riser wires soldered into notches in the edges of the wafers. The modular stages then mount on etched copper base plates which serve again to interconnect and support the several units comprising an electronic subassembly.

An exhaustive discussion of these materials and fabrication techniques is without the purpose of this paper, and the reader is

referred elsewhere [1-4].

2. Inductance in the Module

The module places serious restrictions on the incorporation of inductance into circuits to be realized in this form. The inductance obtainable from a printed or etched flat spiral coil is too small for most practical applications. The space available in the module for conventional coils is, furthermore, not large; the free space between wafers is one-eighth inch while the usable area on a wafer is of the order of one half square inch. Moreover, where the circuit calls for the incorporation of several inductances in the same module, the close physical proximity of these coils may well be expected to lead to difficulty with undesired coupling between them.

3. Modular Delay Lines

With regard to the above considerations, the problem of realizing a lumped parameter delay or pulse-forming network in modular form is particularly difficult. The inductances required are, for the most part, large, and many of them must be mounted within the restricted volume of the module. Furthermore, the experimental trimming of capacitances and couplings for optimum performance, common in delay line development, is virtually impossible to effect once the module has been completely assembled.

This investigation, then, addressed itself to the modular delay line problem along two concurrent lines: (1) a theoretical evaluation of the inductance boundaries within which the module constrains the designer to work (configuration effects), and, (2) an effort to

refine the theory wherefrom delay line design equations derive, in order that the designer may more accurately predict performance prior to construction. Good experimental confirmation of both theoretical approaches was obtained, and the resulting design techniques have been reduced to a readily usable graphical form.

CHAPTER II

DELAY LINE THEORY

1. Delay

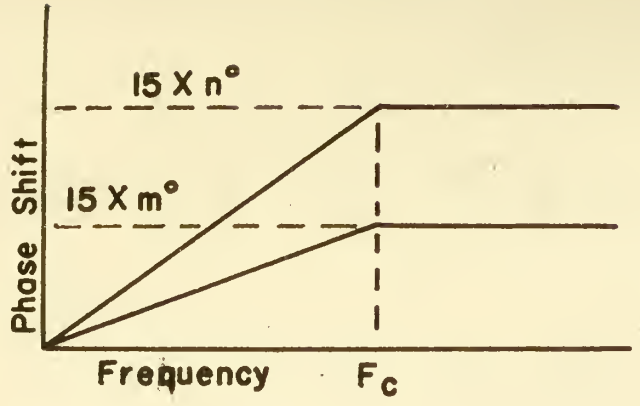
The use of a lumped-parameter L-C low pass filter to afford time delay for electrical signals has become an established technique in many electronic equipments. Ideally, the low-pass filter exhibits a phase-shift versus frequency characteristic which is linear over the pass band of the filter. The ultimate phase shift - i.e., at the cut-off frequency and outside the pass band - is constant and determined by the rate at which the filter cuts off in the following fashion:

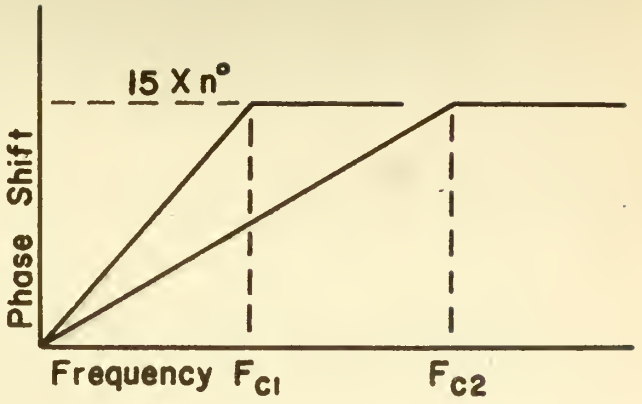
$$\phi_{max} = 15^{\circ} \times \text{(rate of cutoff in decibels per octave)}$$

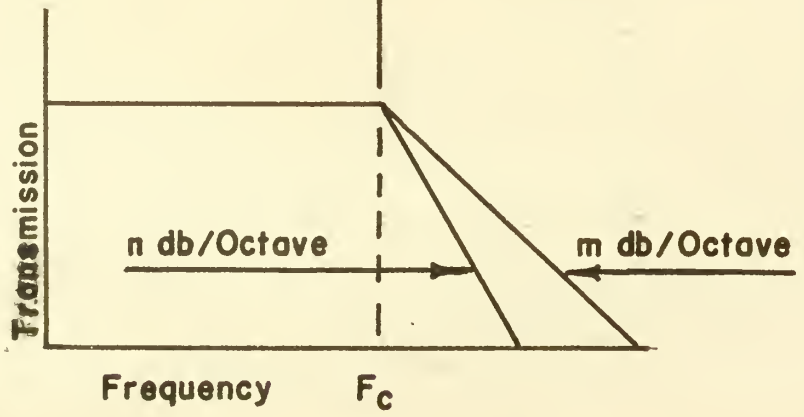
Figure 1 illustrates this behavior.

The product of the phase shift at a given frequency, expressed as a fraction of a complete cycle (360°), by the period of this frequency gives the time by which a signal of this frequency is delayed in progressing through the filter. If, then, the phase shift is proportional to frequency (inversely proportional to period), it follows that signals of any frequency within the pass band of the filter will be delayed by the same time.

In this light, consideration of Figure 1 shows one of the basic properties of the low-pass filter used as a constant delay device: that for a given cutoff characteristic, the delay at any frequency within the pass band of the filteris inversely proportional to the cutoff frequency thereof. Viewing the entire delay structure as







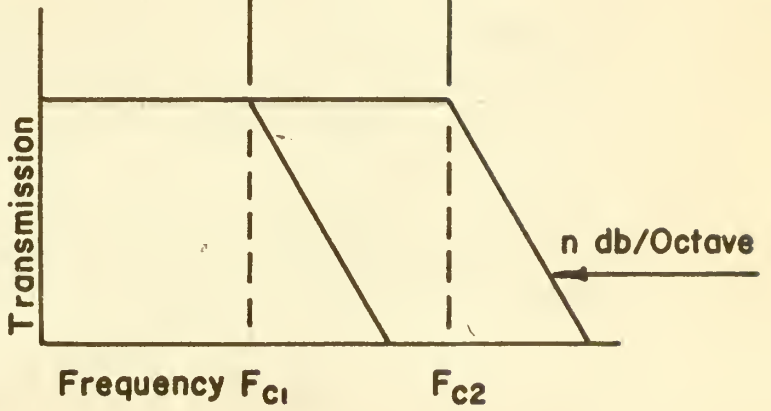


Figure 1

Transmission and Phase Behavior of a Low-Pass Filter

composed of a number of identical "sections", the above may be restated:

> Delay per section is inversely proportional to cutoff frequency.

The factor of proportionality depends on the circuit configuration of the section. The delay afforded by the entire structure may be varied in discrete increments by similarly varying the number of sections of which the network is composed - i.e., the total delay is given by the product of the delay per section by the number of sections.

Viewed in another way, the addition of successively more sections increases in discrete increments (equal to the rate of cutoff per section) the rate of cutoff of the complete structure, and hence the ultimate phase shift thereof. For a given cutoff frequency this accordingly affects the slope of the phase-shift versus frequency characteristic and so the overall delay. Reference to Figure 1 will clarify these basic concepts.

2. Rise Time - I

The constancy of the delay as a function of frequency afforded by the low-pass filter well suits it to the problem of delaying pulse type signals, which contain not one, but many (in principle infinitely many) frequency components. Some consideration must, then, be given the effect of the low-pass filter in substantially eliminating all frequency components of a pulse which lie outside its pass band. The well known Fourier Integral result will serve, at least approximately, to demonstrate the desired trend:

$$\text{Rise time} = 1/2 \times (\text{cutoff frequency}) \quad \text{(Approx.)}$$

Rise time is here interpreted to mean that length of time required

for the output of the delay network to change from some small percentage to some large percentage (usually taken as 0-10% and 90-100% respectively) of its final amplitude when a perfectly rectangular step of voltage or current is applied to its input. It represents a measure of the distortion incurred by the pulse in traversing the delay network.

3. Overall Performance - I

Unfortunately, both the delay per section and the rise time are inversely dependent on the cutoff frequency of the delay network. Hence, if accurate reproduction of a pulse is required - i.e., a short rise time - it follows that the delay per section must be correspondingly small, and that for a specified total delay, the number of sections becomes large.

4. Rise Time - II

In a more sophisticated analysis, some consideration must be given to the effect on overall rise time of cascading successively more sections, as the foregoing indicates will commonly be the case. Regarding the fact of a non-zero rise time as being attributable to the attenuation of those high frequency components of a fast pulse that are outside of the pass band of the delay network, two distinct mechanisms may be discerned to operate. First, as the number of sections is increased, the rate of cutoff of the composite delay structure is correspondingly increased. Hence, those high frequency components just outside the pass band which are partially effective in reducing rise time become progressively less so, since more severly

attenuated. Second, the attenuation below but near the cutoff frequency is not zero, due to losses in the section. Thus, with an increasing number of sections, the attenuation in the upper region of the nominal pass band becomes greater, resulting in a lowered effective cutoff frequency.

The former effect might conceivably be amenable to analysis. The latter, however, since dependent on the losses present in a specific section is not subject to evaluation in general. The dependence of coil and capacitor losses on frequency, moreover, would greatly complicate such a calculation, even for known components.

Despite the apparent intangibility of the problem, it was nevertheless felt imperative to obtain some reasonably quantitative evaluation of the effect on overall rise time of cascading sections. The following approach, details of which are presented in Appendix I, was adopted. The output response of a single section to a step function input was idealized in the form of a function having constant slope for a time T_{r1}, the rise time of the single section, and constant thereafter. In terms of these, a transfer function for a single section readily evolves, and successive operations by this on the step input enables the output waveform to be calculated after any desired number of sections. The result of this analysis is:

$$T_r = T_{r1} N^{(1/3)}$$

Where: T_{r1} = rise time of one section

N = number of sections

T_r = rise time of an N-section network

This result is given in the literature [5], although without substantiation.

5. Overall Performance - II

A straightforward Laplace Transform analysis of a resistively terminated section yields:

$$T_{r1} = 1/2.9 \times (\text{cutoff frequency})$$

Using this result, the following expression, derived in Appendix II, evolves to describe the performance of an N-section lumped parameter delay line:

$$T = (1.2N^{(2/3)} + \tfrac{1}{2})T_r$$

Where: T = total delay

N and T_r as before

This quantitatively expresses that, subject to the constraint of a constant (specified) rise time, the total delay of a multisection delay network increases slower than proportionately to the number of sections incorporated therein. Since the rise time of an N-section line is longer than that of one section, the rise time per section hence the delay per section must correspondingly be reduced when cascading sections.

6. Circuit Configuration of the Section

Consideration has been accorded to this point primarily to the idealized linear phase-shift structure, this in order to establish fundamental relationships which pertain to the delay network problem.

In physically attainable low pass filters, however, the phase-shift versus frequency characteristic is not linear - i.e., the time delay of the network is not constant over the entire pass band. The result is further distortions of the pulse response beyond those demonstrated by the idealized theory. One aim of the designer of a delay network is, therefore, to evolve section configurations which minimize these abberations.

The constant-k prototype filter, while attractive from the standpoint of simplicity, is far from this in consideration of the marked departure from constancy of its delay versus frequency characteristic. Kallman [6] shows this characteristic and it will be noted that the delay error for the constant-k (m = 1) section is approximately 20% at a frequency of 0.5 the cutoff frequency, and becomes progressively worse above this. For the somewhat more complex m-derived section, with m in the range from 1.27 to 1.4, the delay is constant within comparable limits over a much greater portion of the pass band - approximately 0.8 of the cutoff frequency.

Fortunately, sections having values of m greater than unity are physically realizable through the relatively simple expedient, in principle, of allowing positive mutual inductance to exist between the coils. Furthermore, with modular construction it would undoubtedly prove uneconomical from a space utilization standpoint to attempt to reduce the coupling between coils to the extent that constant-k sections were realized. This coupling, on the other hand, could well be used to achieve the performancewise superior m-derived section, with the incidental advantage of better utilization of the available

modular space obtaining from the closer disposition of components.

CHAPTER III

INDUCTANCE CONSIDERATIONS

1. General

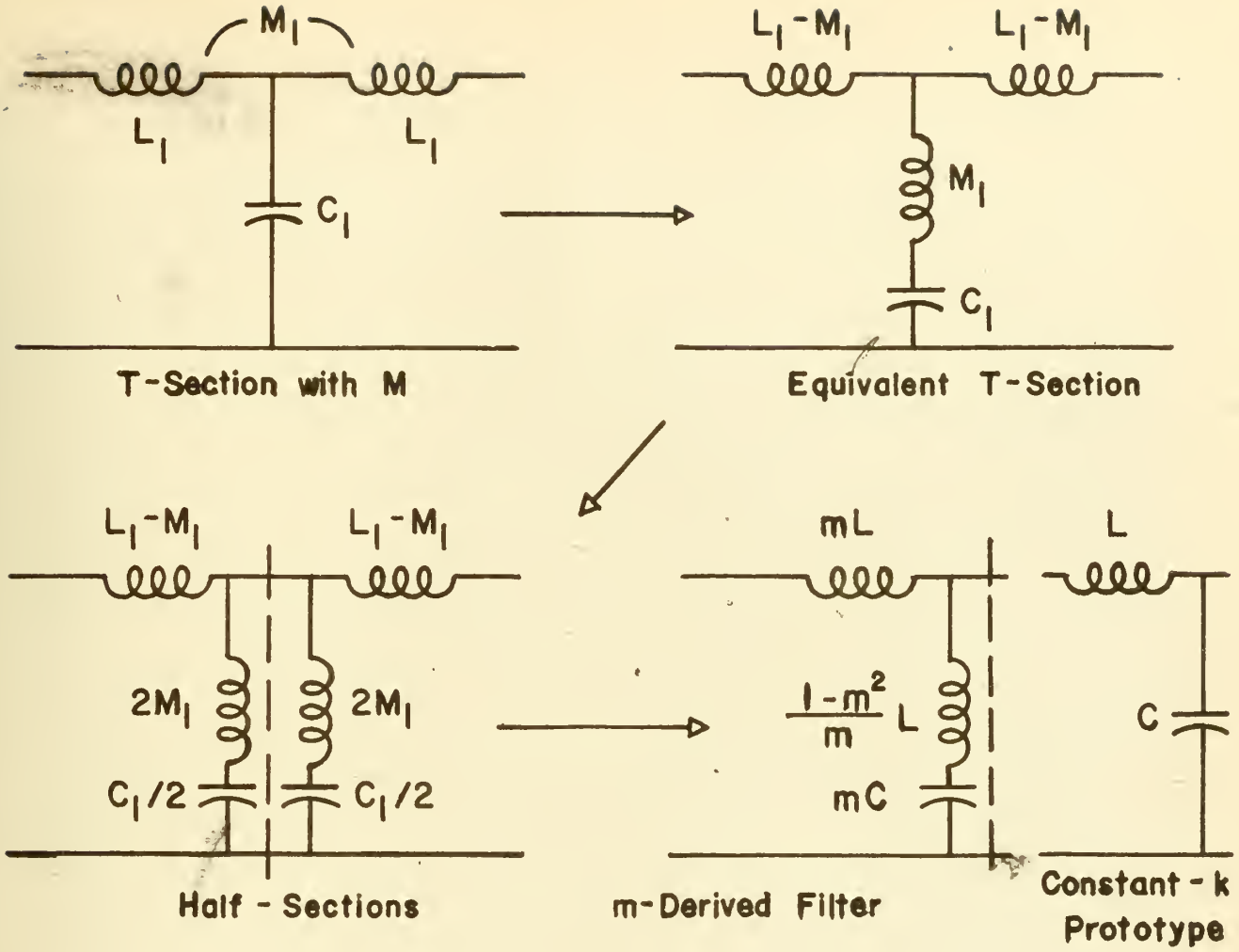
Having elected to concentrate on an m-derived "T" section circuit configuration, the investigation addressed itself to the proposition of discovering a family of coil geometries which provided the correct coupling while also enabling a usable range of inductance values to be obtained. The outstanding limitation here is that the one factor, spacing between coils, which most affects the coupling between them is fixed at certain discrete values by the module itself. Some variation in other coil dimensions must, however, be expected if a range of inductance affording sufficient design flexibility is to be realized.

2. Inductance Calculations

The number "m" which is used in the m-derivation of a filter section from the prototype constant-k section (see Figure 2), and which appears as a parameter in the delay versus frequency characteristics, is related to the coupling coefficient between the two coils (L_1) of a "T" section in the following fashion:

$$\text{Coupling coefficient} = k = \frac{m^2 - 1}{m^2 + 1} \qquad \text{(III-1)}$$

Corresponding to the desired mean value of $m = 1.3$, the required value of coupling coefficient is: $k = 0.256$. As a practical matter, values



$$f_c = 1/2\pi(LC)^{1/2}$$

$$Z_o = (L/C)^{1/2}$$

$L_1 - M_1 = mL$ $\qquad$ $C_1/2 = mC$

$2M_1 = \frac{1-m^2}{m}L$ $\qquad$ $\therefore C_1 = 2mC$

$\therefore L_1 = \frac{1+m^2}{2m}L$

$$f_c = \frac{(m^2+1)^{1/2}}{2\pi(L_1C_1)^{1/2}}$$

$$Z_o = \frac{2m(L_1/C_1)^{1/2}}{(m^2+1)^{1/2}}$$

Fig. 2

Development of m-Derived Delay Line Section

of coupling coefficient in the range 0.24 to 0.28 are satisfactory.

The self inductance of a coil and the mutual inductance between two coils may be written respectively in the following generalized form:

$$L = N^2 \times (\text{some function of geometry only})$$

$$M = N_1 N_2 \times (\text{some function of geometry only}) = N^2 \times f(\text{geometry})$$

where the coils are identical and N refers to the number of turns on a coil. Thus the coupling coefficient may also be written generally:

$$k = \frac{M}{L} = \frac{N^2 \times f_1(\text{geometry})}{N^2 \times f_2(\text{geometry})} = \text{a function of geometry only}$$

This quantity then appears to be the logical choice for a dependent variable in examining configuration effects, as it bears directly (equation III-1) on the electrical conditions to be established and is itself a function solely of the mechanical properties involved. Computation of the coupling coefficient was effected by taking the ratio of the normalized self and mutual inductances, L/N^2 and M/N^2 respectively. This procedure obviates the need to consider specific coils while allowing standard inductance formulae to be used.

Multilayer coils having an axial depth of 1/16 inch were selected for consideration. The radial depth was treated as the independent variable, and the inside diameter entered as a parameter. The following formula, due to Wheeler, is given by Terman [7] for the self inductance of a multilayer coil, and was used in the computation of normalized self inductance for a series of coils.

$$L = \frac{0.8a^2N^2}{6a + 9b + 10c} \quad \text{microhenries}$$

Where: a = mean radius of coil, inches
b = axial depth of coil, inches
c = radial depth of coil, inches

One interesting and convenient feature emerged from this process: that the value of normalized self inductance is practically constant with respect to variations in radial depth, over a wide range. This behavior has been verified experimentally.

For the calculation of normalized mutual inductance M/N^2, the individual coil dimensions were treated as before, and the center-to-center spacing between coils was selected as 1/8 inch. Grover [8] gives the following formula, which was used here, for the mutual inductance between two identical multilayer coils:

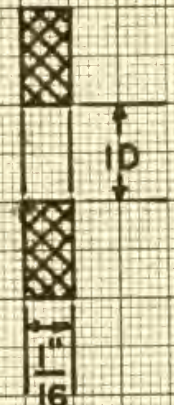
$$M = N^2 M_o$$

where M_o is the mutual inductance between the two single turn central filaments of the coils and is calculated with the aid of tables [8]. More precise methods exist, [7], but the computational labor thereby involved would have been prohibitive for this investigation. The normalized mutual inductance was found to exhibit a variation with radial thickness. Accordingly it is possible to select coil geometries to afford a desired value of coupling coefficient, within limits.

3. Experimental Results

Figure 3 shows the calculated variation of normalized self inductance with the inside diameter parameter; as previously noted, this

Fig. 3
Normalized Self Inductance
vs. Inside Diameter for
Multilayer Coils.



ID - Inches

0.3
0.28
0.26
0.24
0.22
0.2
0.18
0.16
0.14
0.12

L/n^2 - Normalized Self Inductance - Microhenries per $(Turn)^2$

.006 .007 .008 .009 .01

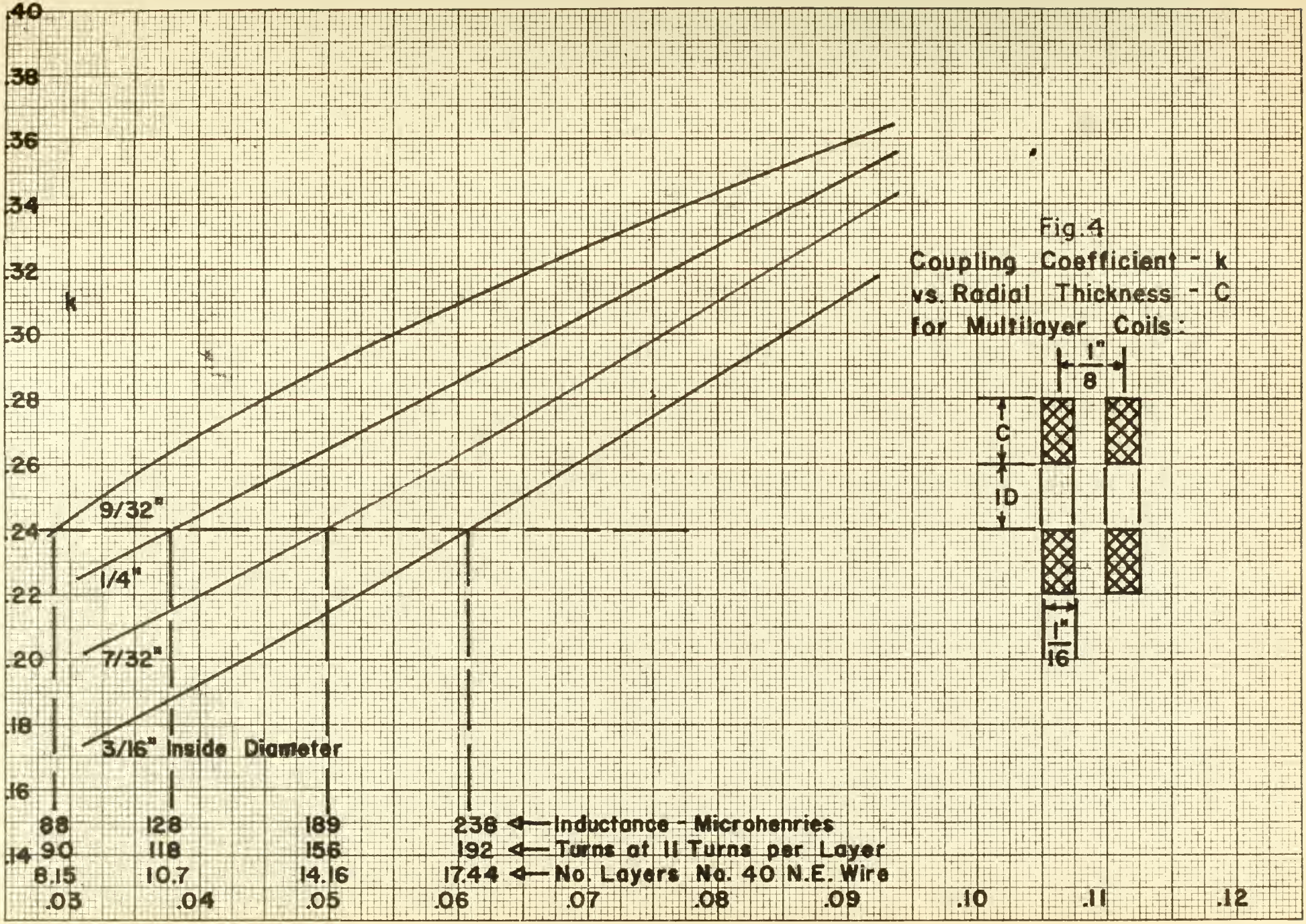


Fig. 4
Coupling Coefficient - k
vs. Radial Thickness - C
for Multilayer Coils.

quantity is practically independent of radial depth over the range of geometries investigated. Figure 4 summarizes the results of the coupling coefficient calculations. As indicated on this Figure, a series of coils was selected to be wound to give a coupling coefficient of 0.24, for the purpose of obtaining direct experimental comparison with the theoretical computations. Table I presents the outcome of this comparison.

TABLE I

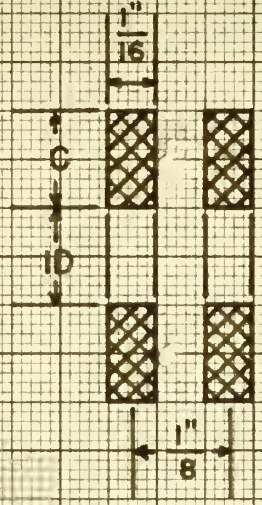
Inside Diameter Inches	Radial Depth Inches	Self Inductance Predicted	Self Inductance Measured	k Predicted	k Measured
9/32	0.0285	88 uh	100 uh	0.24	0.285
1/4	0.0375	128 uh	136 uh	0.24	0.256
7/32	0.0495	189 uh	182 uh	0.24	0.243
3/16	0.061	238 uh	234 uh	0.24	0.238

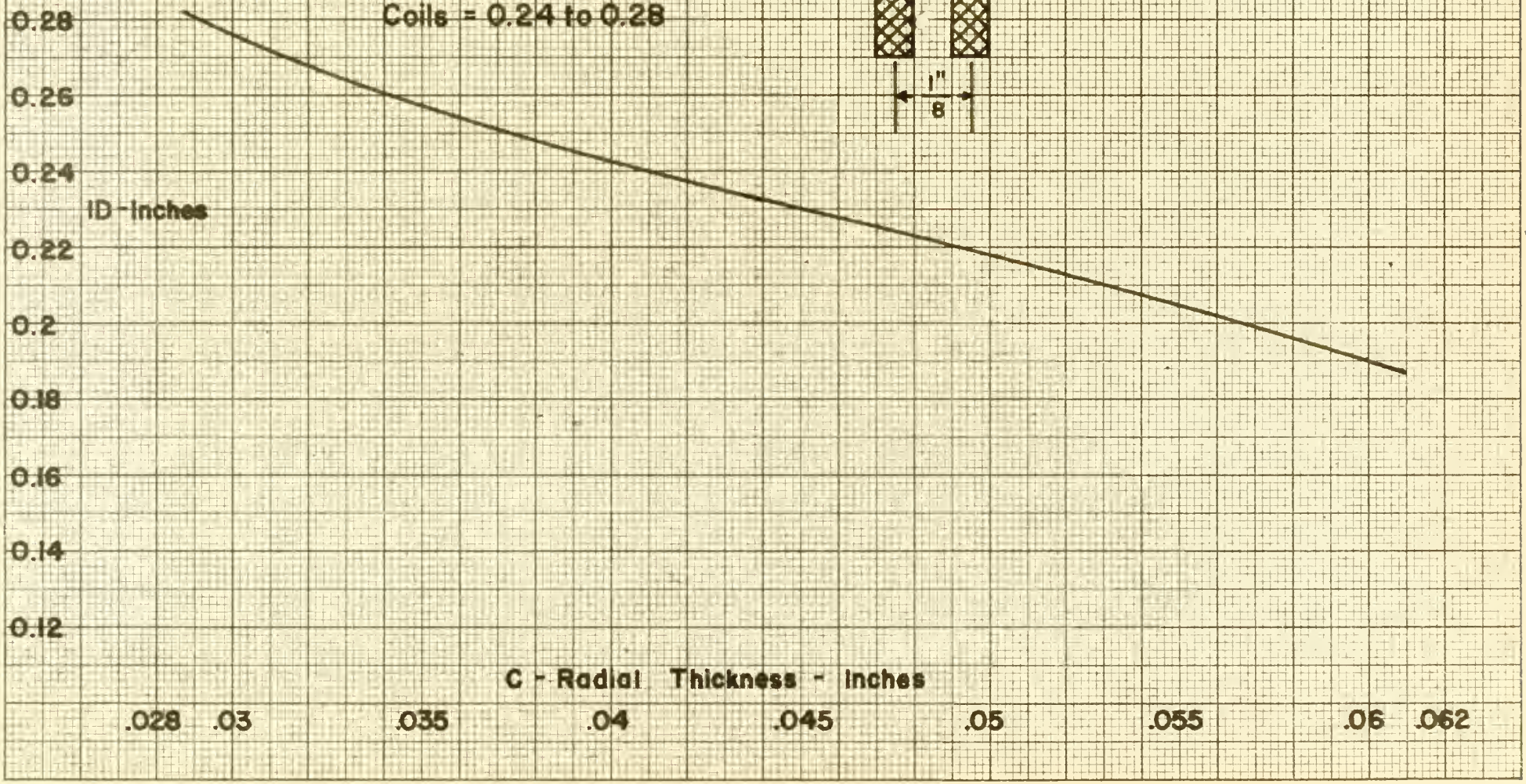
The agreement between the predicted and measured quantities is quite good in all but the 9/32 inch inside diameter case, but even here the agreement is satisfactory. In this instance the axial depth of the coils as wound was 0.01 inch undersize and this can account for the discreptancy. A shorter coil will have greater self inductance; also two such coils when mounted with 1/16 inch spacing between adjacent faces (on opposite sides of the same wafer) will effectively be spaced more closely than the desired 1/8 inch center-to-center, hence a higher coupling coefficient.

Figure 5 summarizes the geometrical relationship which must be maintained between inside diameter and radial depth for the correct

Fig. 5

Radial Thickness vs. Inside Diameter for Coupling Coefficient Between Multilayer Coils = 0.24 to 0.28





coupling coefficient to exist between the coils. In the light of the above results, its use for design purposes is adjudged to be entirely acceptable. A considerable extension of the range of self inductance values obtainable may, of course, be accomplished by changing the number of turns that are fitted into this winding cross section required to give the proper coupling coefficient.

CHAPTER IV

MODULAR CONFIGURATION

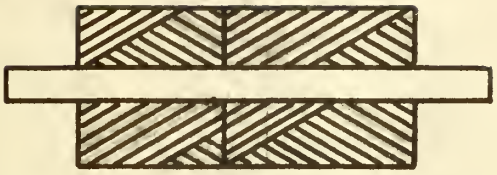
1. Introduction

At this point is is appropriate to turn to a consideration of modular design factors. This has purposely been deferred as it is felt that greater significance will accrue hereto by following the presentation of details pertinent to the theoretical computations upon which such evaluations are based.

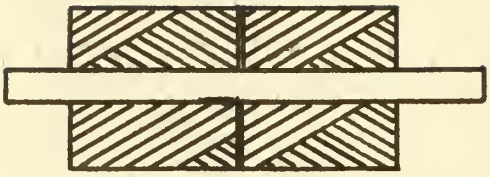
2. Coil dimensions

The 1/16 inch axial depth dimension was selected since such a coil will fit readily into the 1/8 inch free space between wafers in the module, and allow in addition adequate room therein for two ceramic capacitors of the type used in modular construction. A thinner coil was not used as no further economy of space utilization would result therefrom (the matter of connections limits the number of capacitors that can be mounted on one side of a wafer to two). Moreover, winding thin coils is a difficult and tedious process at best, undesirable from the standpoint of production ease and component uniformity.

The 1/8 inch center-to-center spacing was selected since it corresponds to 1/16 inch coils mounted on opposite sides of the same wafer, which itself is 1/16 inch thick. Using this spacing, two coils may be mounted side by side on both sides of the same wafer - four coils per wafer. See Figure 6. Thus, in three wafers four sections can be constructed, where the extra wafer mounts the necessary four capacitors.



4 Coils/Wafer



8 Coils/Wafer

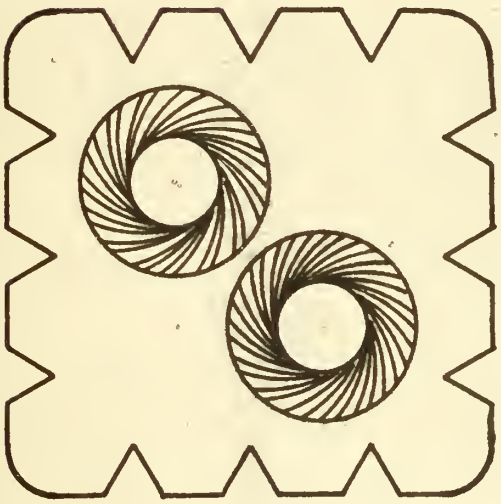


Figure 6

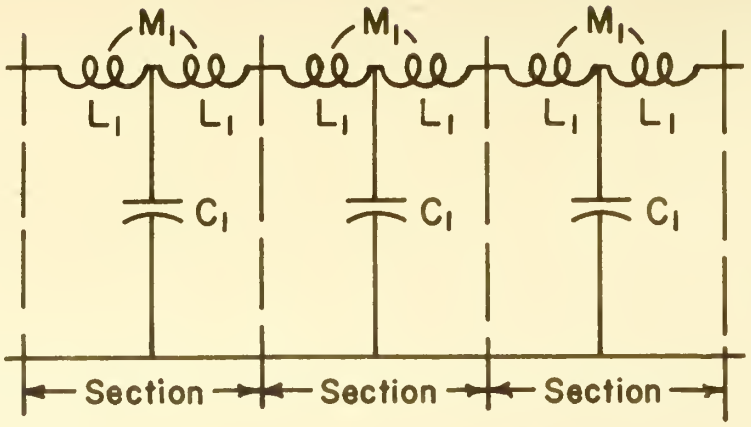
Modular Arrangements for Inductors

Aside from efficiently utilizing the available space, this modular design adapts itself well to the electrical configuration: coils mounted coaxially may readily be designed from the foregoing procedure to have the required value of coupling coefficient k = 0.24 to 0.28. Coils not coaxially arranged have been determined to have only very small coupling between themselves, as is required to be the case between concurrent sections. All the coils, furthermore, are identical.

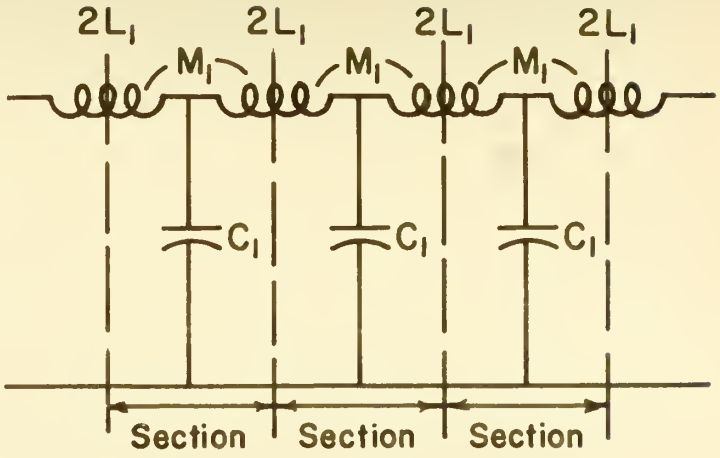
3. Modular Design Factors

The reader may at this point note, as is indicated in Figure 7a, that two physical coils are employed per section, these having the requisite coupling coefficient $k = M_1/L_1 = 0.24$ to 0.28. This appears initially to be something of an extravagance, since a combination, into one, of the two coils L_1 in concurrent sections would result in almost a twofold reduction of the number of inductance components. See Figure 7b. The self inductance of this single coil would, however, be $2L_1$, while the mutual inductance between these coils must remain at the value M_1. Accordingly the coupling coefficient between such coils must be reduced by a factor of two - i.e., $k' = M_1/2L_1 = 0.12$ to 0.14. Reference to Figure 4 shows that this small value of coupling coefficient cannot be realized with reasonable coil dimensions nor range hereof where the center-to-center spacing between coils is 1/8 inch. Thus the spacing between coils must be increased, with resultant sacrifice in effectiveness of modular space utilization.

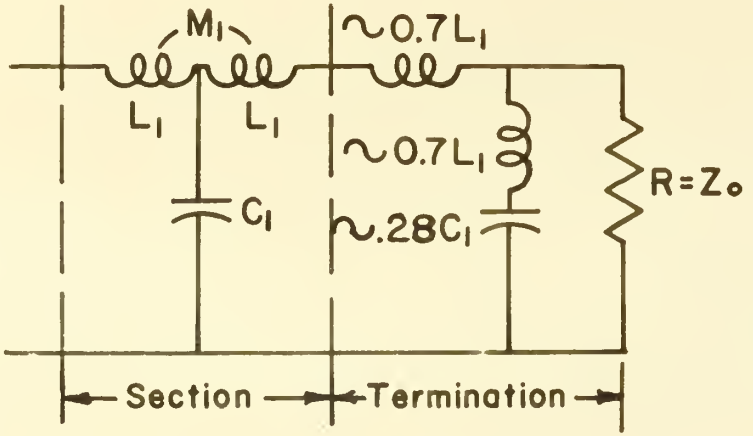
Coils of $2L_1$ inductance, would have to be at least as far apart as on corresponding sides of adjacent wafers, the next possible spacing



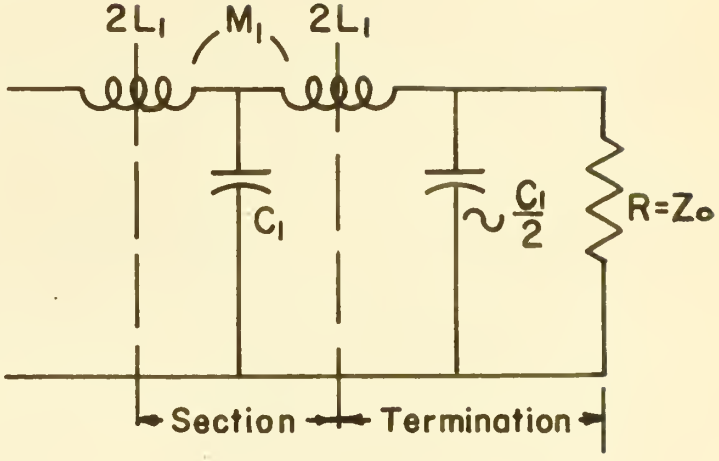
(a) 3 Sections, 2 Coils per Section



(b) 3 Sections, "Lumped Coils"



(c) m-Derived Termination



(d) Constant-k Termination

Fig. 7 Line Configurations and Terminations

allowed by the module. Referring again to Figure 7b, it will be noted, however, that coupling k = 0.12 to 0.14 is required to exist between adjacent coils all the way along the line. The side by side arrangement, two coils per wafer side, with the very small coupling coefficient characteristic of this disposition is, accordingly, no longer suitable. Thus, a coaxial arrangement, one coil per wafer is required. Assuming that the reverse sides of the wafers accomodate the line capacitors, four sections now occupy five wafers (instead of three) even though the number of coils has been reduced from eight to five.

4. Other Comparisons

Several secondary complications also arise in connection with this latter "lumped coil" modular design which are either much smaller or entirely absent in the former two-coil-per-section scheme. The presence of the capacitors between the coils affects the coupling coefficient, as well as the self inductance and "Q" on account of the shorted turn that the capacitor plates present to the magnetic field of the coil. The magnitude of these effects would be extremely difficult to assess beforehand with acceptable accuracy, even for given coil and capacitor dimensions, although this has been observed to be most serious when the coils and capacitors are mounted coaxially, and appreciably less so when the metal of the capacitors intercepts only one side of the coil field. This would be the case where the coils are not centrally located on the wafer as in the two-coil-per-section configuration. The effect of the capacitors on the coupling coefficients would furthermore here be zero, since these components are not mounted

between those coils which it is desired to couple.

Secondly, the end coils of the "lumped coil" configuration have only half the inductance of the center coils. This, while inconvenient from the standpoint of not having identical components throughout, creates additional complications insofar as the coupling between the end coil and that adjacent is concerned. The same value of mutual inductance M_1 must prevail all along the line; the coupling coefficient associated with the end coils must then become:

$$k'' = M_1/(L_1 x 2L_1)^{\frac{1}{2}} = M_1/L_1\sqrt{2}$$

$$= 0.707 x 0.256 = 0.188$$

This different coupling coefficient could be achieved either by altering the dimensions of the end coils relative to the center coils, or by using a different spacing out to the end coils, or both.

5. Conclusion

The foregoing demonstrates how a mere effort to minimize the number of coils in a modular delay line actually leads to the reverse of the intended effect insofar as efficient utilization of space is concerned, as well as introduces secondary effects of a deleterious or inconveniet nature. On the other hand, the use of two physical coils per section to form a line of cascaded m-derived T-sections while far from being an intuitively evident approach appears to constitute the optimum solution to the problem of realizing a lumped parameter delay line in modular form.

CHAPTER V

TERMINATIONS

1. Introduction

The matter of terminations might more appropriately have been taken up in Chapter II under theory. The type of termination most conveniently used, however, depends to some extent on the modular configuration; accordingly this section follows the consideration of modular design factors of Chapter IV.

2. General

The simplest termination for a lumped parameter delay line consists merely of a resistance equal to the characteristic impedance of the filter connected across each end. It is well known, however, that the image (characteristic) impedance of a filter section is neither constant nor resistive in the vicinity of the cutoff frequency. To ameliorate this situation with regard to properly terminating the end sections, it is common practice to incorporate "matching sections" between the main portion of the line and the terminating resistance. Such matching sections may be either of the constant-k or m-derived type.

3. Constant-k Matching Section

For the sake of completeness this type of terminating section will be considered with reference to the "lumped coil" configuration, with which it is most conveniently used. The difficulty with providing a different coupling coefficient between the center and end coils (section IV-4) may be circumvented by winding end coils also of

inductance $2L_1$. The outer half of this coil (see Figure 7d) in conjunction with a shunt capacitor:

$$C_{end} = \frac{1 + m^2}{4m} C_1 = 0.571C_1 \; ; \; m = 1.3$$

will then form a constant-k half section of the same characteristic impedance as the m-derived center sections. A resistor equal to this characteristic impedance should then be connected across C_{end} to complete the termination.* It should be mentioned that a delay line of this type, so terminated, consists of a number of sections equal to the number of coils, one section of which is of the constant-k type (the sum of the two end half sections), the remainder of which are of the m-derived type.

4. Terminations for T-Section Line

The constant-k matching section may, of course, be used with the T-section (two-coil-per-section) delay line as well as with the "lumped coil" variety. There is, however, one important difference: the coil associated with the matching section cannot conveniently be lumped with the end coil L_1, as is the case in the latter instance. Were this done, the inductance of the end coil would be greater than L_1, and a coupling coefficient smaller than k = 0.24 to 0.28 would have to be provided between this coil and the adjacent coil L_1 in order to maintain the correct value of mutual inductance M_1. The resultant complication of the design is an obvious disadvantage.

* Moskowitz and Racker [5], who treat this type of delay line recommend a "half-size" capacitor (which is close enough to the figure 0.517) in parallel with a resistor equal to the characteristic impedance as a terminating device.

Since a physically separate coil, with its associated wafer must be provided for the matching section, the possibility arises for use of a more elaborate m-derived matching section. See Figure 7c. Such a device should have a value of m less than unity, which requires the use of two coils for physical realization. This is, however, no disadvantage from the standpoint of expenditure of modular space. The two terminating coils may always be mounted side by side on one side of the wafer accommodating the terminating components, since their inductance, hence physical size, is smaller than that of the line coils which are themselves so mounted. Due to this coplanar disposition, the coupling between the terminating coils is negligible; the reverse side of their wafer can readily mount the one capacitor which is necessary in either type matching section. The value of m chosen for the m-derived matching section is customarily 0.7, as this allows both coils to be identical; a capacitor equal to 0.28 C_1 in series with the shunt coil completes the design for characteristic impedance equal to that of the delay line.

CHAPTER VI

DESIGN AIDS

1. General

It was borne in mind that three fundamental quantities would ordinarily constitute the complete specifications for a pulse delay network: (1) the total delay, (2) the rise time, and (3) the characteristic resistance. It is possible from these completely to derive the necessary circuit configuration.

2. Design equations

The three equations which enable the designer to evolve a network to satisfy the fundamental specifications are derived in Appendix II and will merely be stated here. Cascaded m-derived T sections are assumed, and the nominal value of m is taken as 1.3 since the delay versus frequency characteristic is flattest for this case. The equations are:

$$T = (1.2N^{(2/3)} + \tfrac{1}{2})T_r = XT_r \qquad \text{(VI-1)}$$

Where: T = total delay
T_r = rise time
N = number of sections

This permits a solution for the required number of sections to be accomplished in terms of the first two of the specifications.

$$T = (N + \frac{1}{2.4} N^{(1/3)})\, d = Yd \qquad \text{(VI-2)}$$

Where: T = total delay
N = number of sections
d = delay per section

This permits a solution for the delay per section to be accomplished in terms of the first specification and the number of sections.

$$L_1 = 2.5dZ_o \qquad (VI-3)$$
$$C_1 = d/Z_o$$

Where: L_1 = value of the physical inductor

C_1 = value of the physical capacitor

Z_o = characteristic impedance

This permits a solution to be accomplished for the actual component values that must be fabricated for incorporation into the delay line in terms of the third specification and the delay per section.

3. Nomographs

Nomographs (Figures 8, 9, 10) were constructed for rapid solution of design equations VI-1, VI-2, and VI-3 respectively. A straight line drawn through the specified values of rise time (T_r) and total delay (T) may be extended to intersect the number-of-sections scale (N) on nomograph No. 1 (Figure 8). Since only an integral number of sections is realizable, the next higher integer to the intersection of the line with the N scale should be selected as the appropriate value of N. Choice of the next higher integer rather than the next lower allows some margin of safety in meeting the rise time specification. The scale N is calibrated in unit steps to N = 12, but not beyond. Adjoining the N scale is a scale X, the coefficient of T_r in equation VI-1; this may be used to interpolate the higher range of the N scale; where this is necessary, by solution of the equation:

Delay Line Design Nomograph No. 1

$$T = (1.2\,n^{2/3} + 0.5)T_r$$

$$= X\,T_r$$

$m = 1.3$

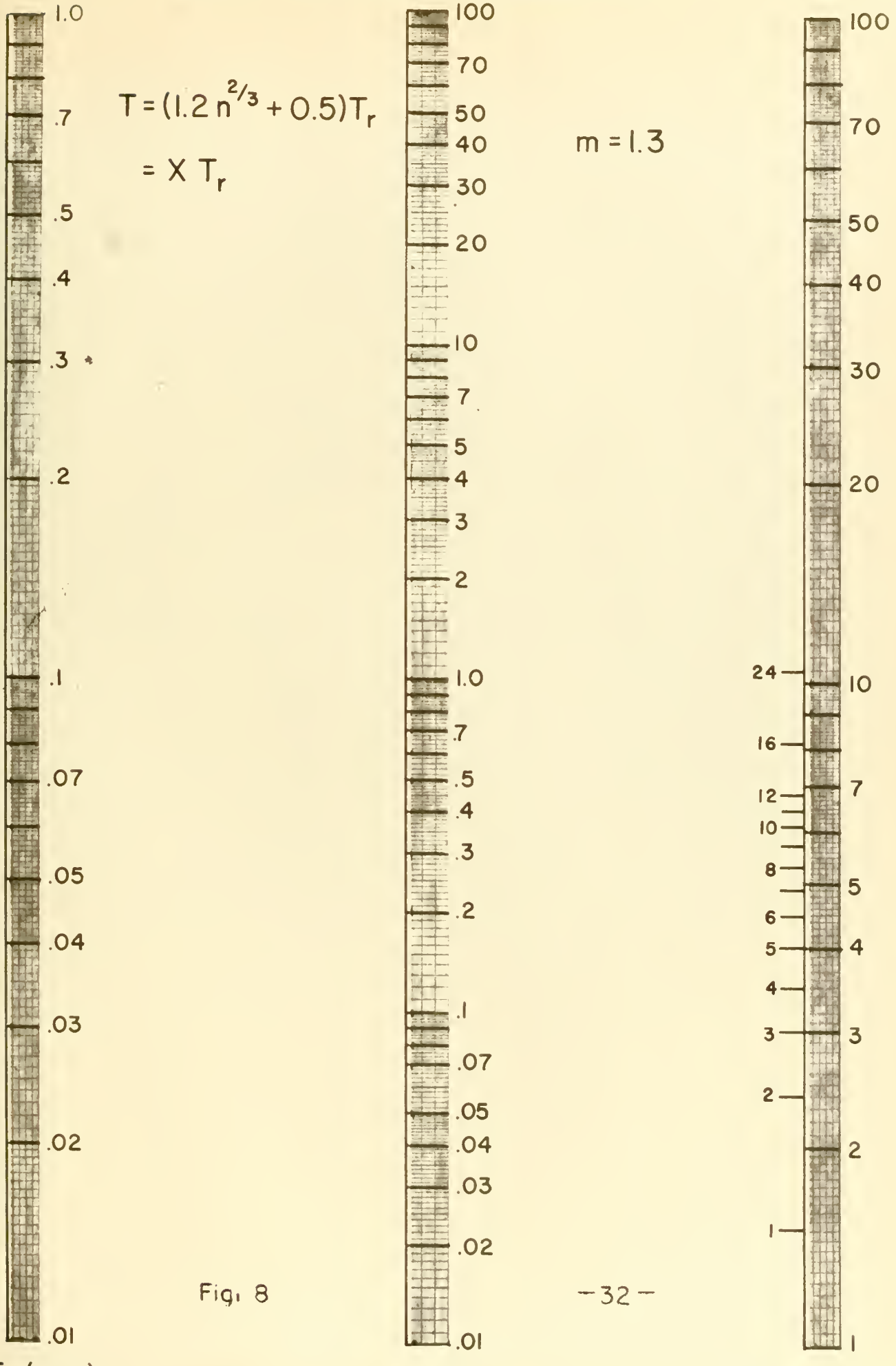


Fig. 8

Delay Line Design Nomograph No. 2

$$T = \left(n + \frac{n^{1/3}}{2.4}\right) d$$

$$= Y d$$

$m = 1.3$

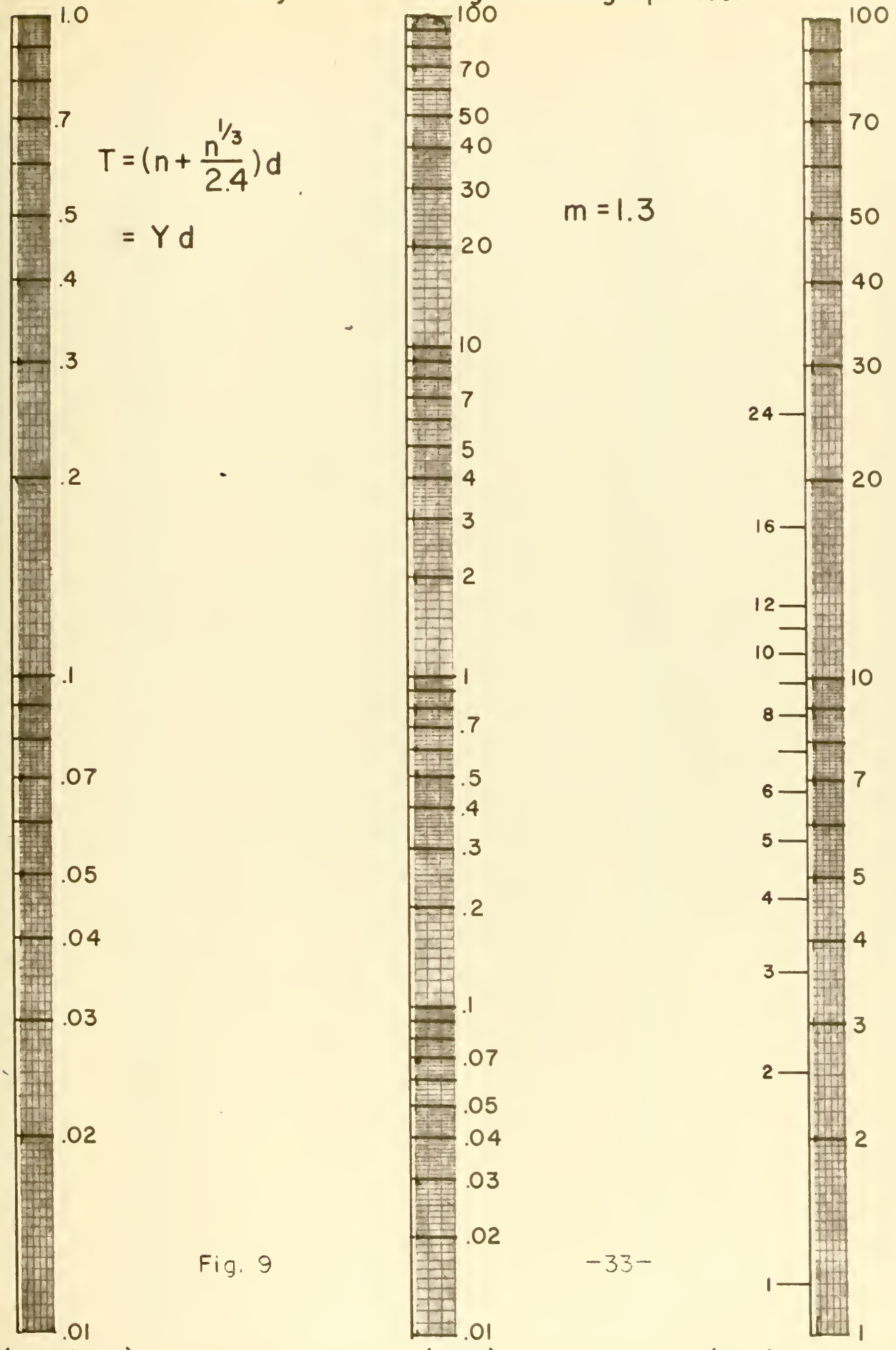


Fig. 9

Delay Line Design Nomograph No. 3

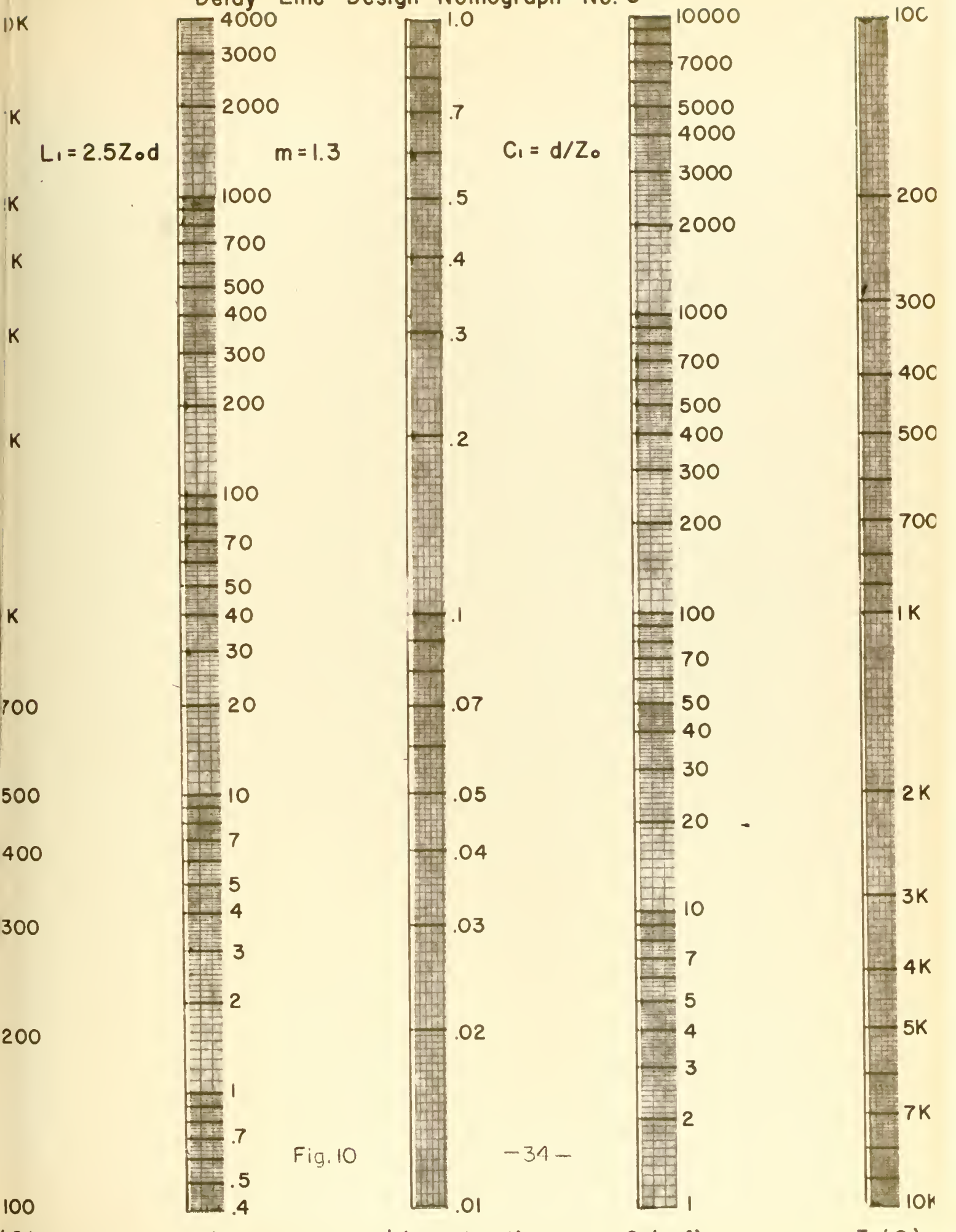


Fig. 10

$$X = (1.2N^{(2/3)} + \tfrac{1}{2}).$$

A straight line drawn through the values specified for total delay (T) and found for the number of sections (N) from nomograph No. 1 may be extended to intersect the delay-per-section scale (d) on nomograph No. 2 (Figure 9). Again the scale of N is calibrated in unit steps only to N = 12; adjacent hereto is an auxiliary scale (Y), the coefficient of d in equation VI-2, which allows interpolation of the higher range of the N scale by solution of the equation:

$$Y = (N + \frac{1}{2.4}N^{(1/3)})$$

Nomograph No. 3 (Figure 10) completes the design procedure by solving for the necessary values of inductance and capacitance. A straight line drawn through the value on the left hand scale specified for characteristic impedance (Z_o), and the value found for delay per section (d) by use of nomograph No. 2 will intersect the inductance scale (L_1) at the required value. Similarly, a straight line drawn through the same specified value of characteristic impedance (Z_o) on the right hand scale and the value found for delay per section (d) by use of nomograph No. 2 will intersect the capacitance scale C_1 at the required value. It should again be pointed out that these are the actual values of the physical components that must be fabricated for use in the delay line, and do not refer to a prototype section.

4. Example

Specifications for a delay line in current use are:

Total delay (T): 0.33 microseconds
Characteristic impedance (Z_o): 1000 ohms
Rise Time (T_r): 0.1 microsecond

The straight line drawn through the values for delay (T) and rise time (T_r) of 0.33 and 0.1 microsecond respectively on nomograph No. 1 extend to an intersection with the number-of-sections scale (N) between three and four. Accordingly, a four section line is chosen. The line drawn through N = 4 and T = 0.33 usec. extends to an intersection with the rise time scale T_r on this same chart at 0.094 usec. Thus some leeway is provided in meeting the rise time specification. Next, the line drawn through the values N = 4 and T = 0.33 usec. on nomograph No. 2 is extended to the delay-per-section scale (d) which it intersects at a value of 0.071 microsecond. At this point, the results of this manipulation may be checked:

4 sections @ 0.071 usec/section	=	0.284 usec
plus $\frac{1}{2}T_r$ of 0.094 usec	=	0.047 usec
Total delay (T) to 50% point	=	0.331 usec

This differs from the specified delay by only 0.3 percent. Finally, the lines drawn on nomograph No. 3 between the specified characteristic impedance (Z_o) of 1000 ohms and d = 0.071 usec intersect the scales of inductance (L_1) and capacitance (C_1) at values of 28.6 uh and 70.6 uuf respectively. Concurrent sections would appear as in Figure 7a.

CHAPTER VII

EXPERIMENTAL CONSTRUCTION AND RESULTS

1. Introduction

Having examined (Chapter II) those factors pertinent to the performance of a lumped parameter delay line, derived (Appendix II) quantitative relationships between these quantities, constructed (Chapter VI) readily usable design aids, and (Chapter III, IV) decided upon the modular configuration giving most promise for simultaneous satisfaction of the electrical and modular space utilization requirements, the investigation was considered in a position to undertake the construction of experimental delay lines. It was anticipated to obtain from tests on such lines, information pertaining to the accuracy of the various design procedures, and to the relative merits of the terminating schemes discussed in Chapter V. The delay line designed in the example (Section VI-4) on the use of the nomographs was first selected for construction.

2. Coil Design

Fundamental to the realization of a modularized lumped parameter delay line, once the component values have been established, is the matter of designing coils (L_1) having the geometry required to give the proper coupling coefficient between themselves: $k = 0.24$ to 0.28. For illustrative purposes, this procedure follows for the case at hand:

(1) 1/4 inch is selected for inside diameter. This choice is

made since the desired inductance (28.6 uh) is less than the smallest tabulated on Figure 4, hence indicating that the desired self and mutual inductance conditions may most easily be achieved with a large inside diameter. An inside diameter of 9/32 inch was not chosen since difficulty was experienced in accurately winding coils of this geometry when the coil design procedure was experimentally verified.

(2) From the values tabulated on Figure 4, it is noted for the radial depth giving k = 0.24 that 118 turns corresponds to 128 uh inductance. The number of turns required to give 28.6 uh is then:

$$N = 118(28.6/128)^{\frac{1}{2}} = \underline{56 \text{ turns}}.$$

Alternatively, using Figure 3, the normalized self inductance L/N^2 equals 0.0092 uh/turn^2 when the inside diameter is 1/4 inch. Therefore:

$$N = (28.6/0.0092)^{\frac{1}{2}} = \underline{56 \text{ turns}}.$$

(3) It is elected to use #36 nylon-enamel wire, the diameter of which is 0.005 inch. From Figure 5 it is noted that the required radial depth is 0.0375 inch. Thus, the number of layers which are to be wound on the coil is:

$$\text{No. layers} = 0.0375/0.005 = \underline{7.5}$$

This number is used to calculate the appropriate coil winding machine gear ratios and the non-integer value is no cause for concern.

(4) Two "crossovers" per turn is selected on the basis of past experience with winding coils of this type. Using the procedure given

in Appendix III, the required mandrel/cam gear ratio is calculated to be 90/84.

3. The Components

Eight coils were wound according to the above design, as required to realize a four-section delay line. Gratifyingly, the mean measured value of inductance of these coils was 29 microhenries, which compares favorably with the desired value of 28.6 uh. Capacitors were fabricated in the usual fashion using a 11/32 inch round pattern on ceramic bodies having a dielectric constant of 66.2, corresponding to a capacitance of 68 uuf. The actual values of capacitance obtained were closely grouped about the value 75 uuf.

4. Modular Layout

A modular design, shown in Figure 11, was evolved consistent with the considerations established in Chapter IV. While m-derived termination matching sections were incorporated herein, they were not connected until after experiments were performed using the simple resistance-only termination.

Note that careful attention must be accorded the matter of coil winding directions and connections when mounting them on the wafers. The coils which it is desired to couple are mounted coaxially on opposite sides of the same wafer, and in order to provide the proper sign of mutual inductance (positive), they must have relative winding directions and connections as though they had been wound from a single length of wire on a common mandrel. This may be accomplished in either of two ways:

PROJECT: *Delay Line*

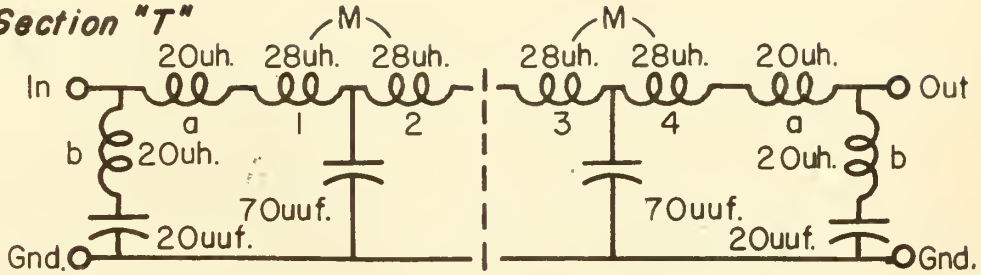
MODULE: *4-Section "T"*

REVISION: *0*

DATE: *8/5/55*

ENGINEER: *Downing*

CIRCUIT DIAGRAM



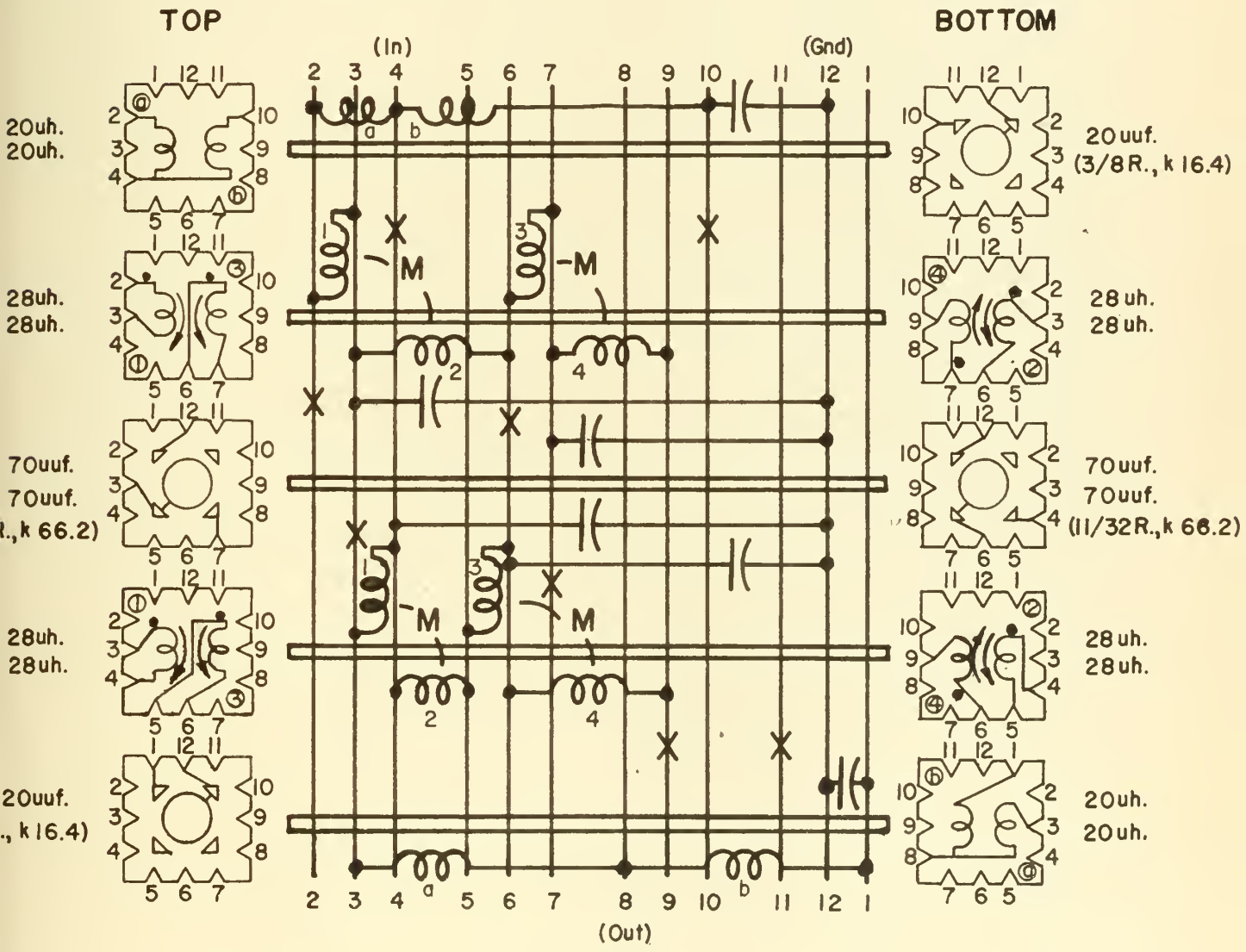


Figure 11
Modular Layout for Delay Line

(1) If when simultaneously viewed along their common axis, both coils are so orientated that they proceed in the same direction (clockwise or counter-clockwise) from outside to inside of the winding, then they must be connected outside (of one coil) to inside (of the other coil).

(2) If when viewed as above, the coils proceed in opposite directions from outside to inside, then they must be connected outside to outside or inside to inside.

On the modular layout sheet (Figure 11) the dotted ends of the coils represent the outside of the winding, and the curved arrows indicate the direction of progression from outside to inside of the winding. Assembly of this proposed delay line module was accomplished in the best Chinese-puzzle tradition.

5. Testing Technique

Figure 12 shows the laboratory set-up used to examine the performance of subject delay line, and is self explanatory. Observations were made of total delay, rise time, and overshoot.

6. Experimental Results

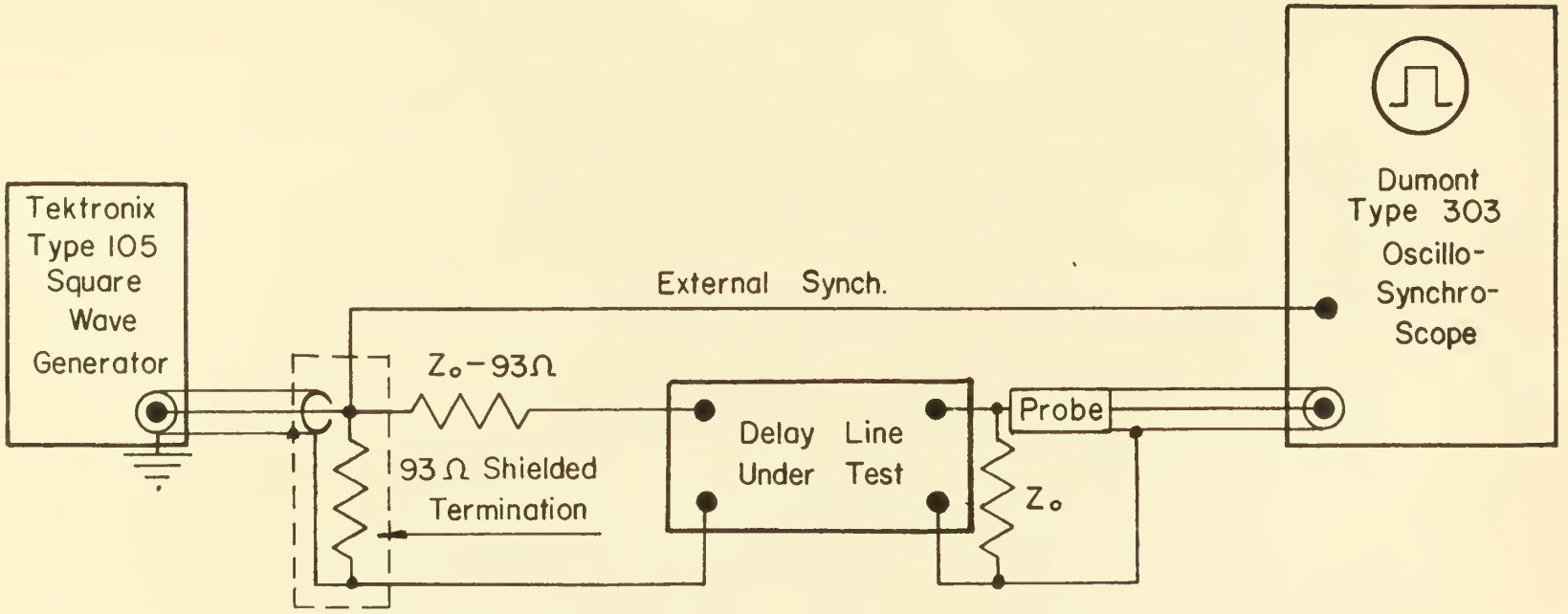
The performance of the line when terminated by 1000 ohm resistors only is as follows:

Total delay: 0.33 microsecond (to 50% point)

Rise time : 0.1 microsecond (10% to 90%)

Overshoot : 5% peak-to-peak, approximately

With respect to total delay and rise time, the agreement with the



Figure

Delay Line Test Setup

specified performance is very good. The reality of the overshoot observations is, however, open to some question. A probe capacitance of 20 uuf is present across the output terminating resistor during the measurement, and this may be expected somewhat to reduce the amplitude of transient oscillations which would otherwise be present. From a practical point of view, however, the application in which a delay line of these specifications is incorporated places a capacitance of this order of magnitude across the output. Hence the performance of this delay line, resistively terminated, is adjudged to be entirely acceptable.

The m-derived termination matching sections, consisting of 20 microhenry coils and a 20 uuf capacitor were then connected and the performance of the line re-examined:

Total delay : 0.38 microsecond

Rise time : 0.1 microsecond

Overshoot : 10% peak-to-peak approximately

As is to be expected, the overall delay is increased somewhat (about 15%) by the incorporation of additional low pass sections. What is more interesting, however, is that the overshoot performance is actually degraded, rather than improved as might be expected to result from a better termination. An explanation of this behavior is not readily apparent except that it may be suspected that the probe capacitance across the output has a greater effect on the resistive termination than on the m-derived termination.

7. A "lumped coil" Delay Line

During the early phases of this investigation, a delay line of the "lumped coil" variety using constant-k termination matching sections was constructed. It is worthwhile from the standpoint of completeness to examine the performance of this network.

The line physically consisted of the following:

Number of sections: 4

Inductance ($2L_1$) : 25 uh

Capacitance (C_1) : 225 uuf

End capacitors : 115 uuf

The coils were coaxially arranged on corresponding sides of adjacent wafers, one coil per wafer, and were so designed as to give a coupling coefficient of approximately 0.12. Due to the presence of the capacitors between the coils the actual coupling coefficient was somewhat less than this, having a value of about 0.1, corresponding to m = 1.2. Thus, from equation (2) of Appendix II the characteristic impedance is in the neighborhood of 500 ohms. Using in order equations (7) and (6) of Appendix II and equation (1) of Appendix I, the rise time is found to be 0.12 microsecond. Considering that three sections of this line have m = 1.2 and one is constant-k (m = 1), use of equations (1) and (5) of Appendix II yields 0.36 microsecond for total delay. Experimentally, these quantities are:

Total delay: 0.34 usec (to 50% point)

Rise time : 0.13 usec (10% to 90%)

Overshoot : 15% peak-to-peak

Considering the approximate fashion in which the effect of the

capacitors upon the coil parameters was taken into account, the agreement here is reasonably good. With respect to overshoot, the results are considered to be a much truer picture than is the case for the T-section line previously discussed. Here the probe capacitance is largely swamped out by the 115 uuf terminating capacitor. Accordingly it appears reasonable to take the 15% peak-to-peak figure quoted as representative of the performance of a constant-k termination matching section.

CHAPTER VIII

CONCLUSION

1. General Theory

The relationships developed in Appendices I and II to describe the overall performance of a multi-section lumped parameter delay line are believed to constitute a valuable refinement of standard delay line design methods. In the case of the delay lines constructed according to this refined technique, excellent agreement was obtained between predicted performance and that measured in the laboratory.

The reduction of these design equations to a readily usable graphical form greatly simplifies the computation of those component values as are necessary to realize a delay line of certain specified characteristics. While these tools apply to only one specific type of line (cascaded m-derived T sections, m = 1.3), it is to be noted that this circuit configuration constitutes the optimum solution to the problem, both as regards obtaining maximum electrical performance - i.e., constant delay over the pass band of the line - and realizing the structure in the mechanical form of a Tinkertoy module.

The experimental results pertaining to the possible improvement of transient characteristics (overshoot reduction) which might result from the incorporation of termination matching half sections at each end of the line indicate that this procedure is of questionable merit. It appears, at any rate, in the case of the T section line, that a small capacitor shunting a resistance-only termination is capable of

cleaning up the transient response of the network to a greater extent than the elaborate m-derived matching section, this with no appreciable effect on the rise time or total delay. Accordingly the design nomographs do not take into account any increase of total delay due to the use of termination matching sections.

2. Modular Configuration

A major portion of the investigation was devoted to the fundamental problem of discovering coil geometries which would permit not only predictable and controllable, but as well advantageous couplings to exist between the numerous inductive components that must here be fitted into the restricted modular volume. A clear definition of that modular configuration that resulted in maximally effective space utilization, consistent with electrical performance, emerged from this study. Information and techniques whereby specific coils may readily be designed and wound for this application also evolved herefrom.

3. Comments on mechanical construction

Reference to Figure 6 will show that some consideration was given the possibility of mounting four coils per wafer side, eight to a wafer, where the outside diameter of the coils permits. This design is essentially identical electrically and configuration-wise to the four coil per wafer arrangement investigated experimentally, and may be expected to perform in a similarly satisfactory fashion. Here, it is possible to realize four m-derived T sections in two wafers instead of three as with the four coil per wafer scheme when the four capacitors required are accounted for. The resultant further efficiency of space

utilization is evident. Unfortunately, time limitations did not permit an investigation into the construction of a modular delay line in this form. Moreover, the large number of riser wires (eight) required alone to interconnect the coils introduces some doubt that sufficient uncut risers can be provided throughout the module to afford an acceptable degree of mechanical rigidity.

In experiments on the modules constructed an observable, though not objectionable amount of direct feed-through was encountered due to capacitive coupling between the riser wires. It is important on this account so to arrange the modular layout that very remote portions of the line are not connected on riser wires closely adjacent, particularly the input to and the output from the line.

In addition to the precautions previously discussed concerning the relative winding directions of the coils, a reasonable amount of care must be exercised to insure that the coils that are to be coaxially disposed actually are so. The axes of these coil pairs should coincide within approximately 0.01 inch in order to insure that the proper coupling coefficient exists between them.

4. Comments on Electrical Characteristics

During the course of experimental observations on the modularized delay lines constructed by this investigation, a certain amount of drift in their performance characteristics was noted. Care was exercised throughout to maintain accurate calibration of the test instruments used, and it is felt that this drift in large measure represents the effect of instability on the part of certain of the

delay line components. In particular, a gradual shortening (by approximately 10%) in the total delay over a period of several days following assembly is attributed to the rapid initial loss of capacitance characteristic of the high dielectric constant ceramic capacitors used in modular construction. Moreover, the relatively large temperature coefficient of capacitance inherent to ferroelectric ceramics may be expected to introduce corresponding short-term instabilities in delay line performance.

5. General

The modular design of electronic equipment owes its existence to the demand for an unsupervised and highly automatic method for fabrication and assembly. Accordingly the maintenance of as close component tolerances as is required for precision delay line applications does not appear to be feasible by this means. An unavoidable distribution of initial component values of the order of 10% plus the subsequent drift characteristic of some of the elements used may well be expected. Where, however, tolerances of this magnitude are acceptable, it is felt that the realization of lumped parameter delay networks in modular form is as readily accomplished as by any more conventional technique.

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APPENDIX I

RISE TIME OF MULTI-SECTION DELAY NETWORK

The output response of a single section of the network to a step function input is idealized in the form of a trapezoidal waveform (see Figure 13), the 0% to 100% rise time of which is taken as T_{r1}, the rise time of the single section. While the sharp discontinuties of this waveform are not physically possible, it is assumed that the elimination of these by subsequent sections will benefit the ability of this analysis to describe the actual situation.

Laplace transforms of these input and output functions are respectively:

$$L\left[e_i(t)\right] = E_i(p) = \frac{1}{p}$$

$$L\left[e_{01}(t)\right] = E_{01}(p) = \frac{1}{T_{r1}p^2}\left[1-\exp(-T_{r1}p)\right]$$

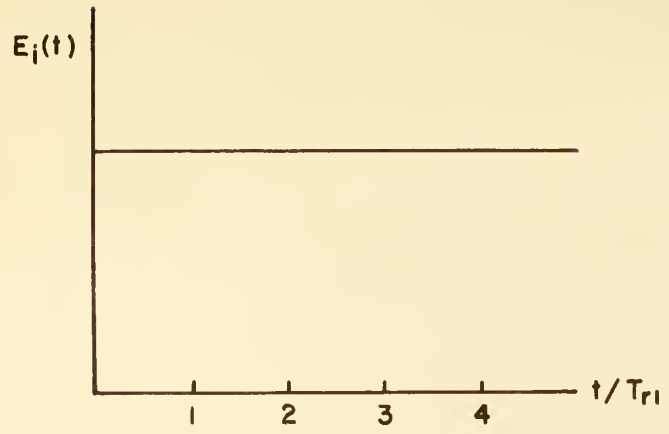
The idealized transfer function of a single section may now be defined as:

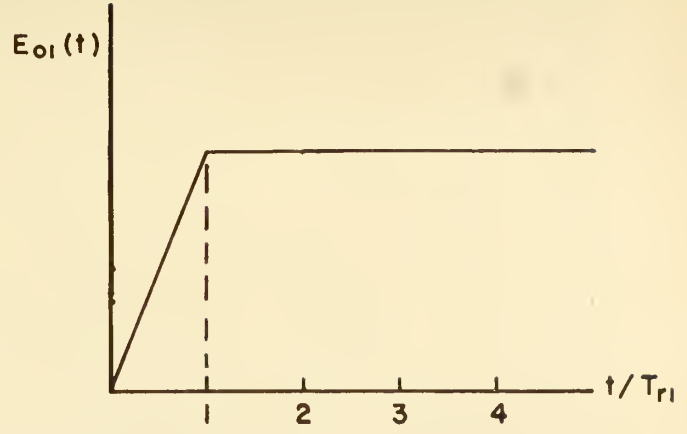
$$R(p) = \frac{E_{01}(p)}{E_i(p)} = \frac{1}{T_{r1}p}\left[1-\exp(-T_{r1}p)\right]$$

If furthermore the input for each succeeding (nth) section is taken as the output of the previous (n-1) one:

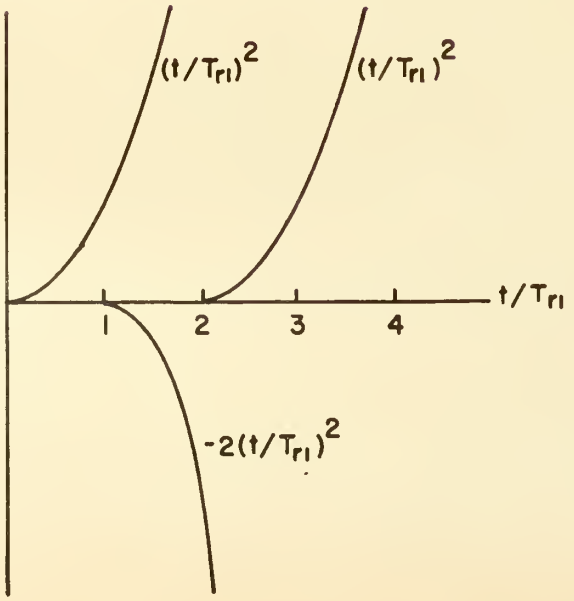
$$E_{o(n)}(p) = E_{i(n+1)}(p) ,$$

it follows that the transformed output of the nth section will be given by:





Components of $n!\,T_{r1}^n e_{on}(t)$ for $n=2$



Components of $n!\,T_{r1}^n e_{on}(t)$ for $n=3$

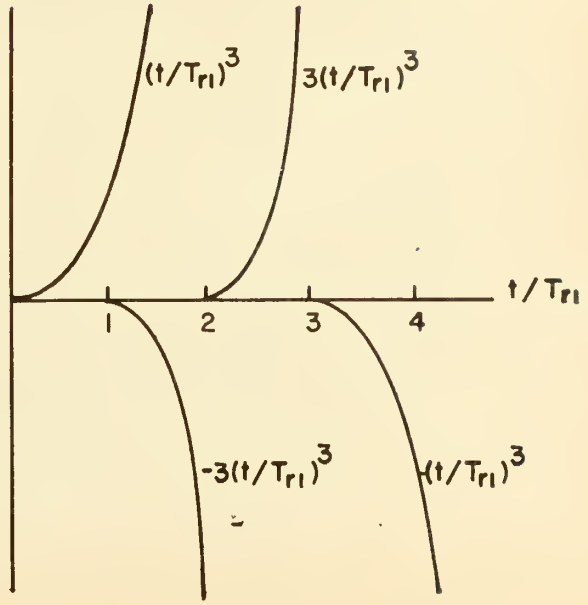


Figure 13

$$E_{o(n)}(p) = \left[R(p)\right]^n E_i(p) = \frac{1}{T_{rl}^n\, p^{(n+1)}} \left[1-\exp(-T_{rl}p)\right]^n .$$

Inversion of this transform yields:

$$e_{o(n)}(t) = L^{-1}\left[E_{o(n)}(p)\right]$$

$$= \frac{1}{n!\,T_{rl}^n} \sum_{i=0}^{(n-k)} (-1)^i\, {}^nC_i\,(t-iT_{rl})^n ;\ (n-k)T_{rl} \leq t \leq (n-k+1)T_{rl}$$

where ${}^nC_i$ represents the binomial coefficients of order n. Figure 13 also shows normalized components of this function for two values of n.

A numerical evaluation of this function and of its first derivative with respect to time (t) (at the 50% point) for values of n from one to 12 indicated that the 10% to 90% rise time (T_r) of an n-section delay network may be taken as:

$$T_r = T_{rl}\, n^{(1/3)} \qquad \text{(AI-1)}$$

APPENDIX II

DELAY LINE DESIGN EQUATIONS

The time delay of an m-derived low pass filter section is given by [5]:

$$d = 2m\sqrt{LC} \tag{AII-1}$$

where the number m is defined in terms of the coupling coefficient (k) between the coils of a T section:

$$k = \frac{M_1}{L_1} = \frac{m^2 - 1}{m^2 + 1}$$

The quantities L and C refer to the inductance and capacitance of the prototype constant-k half section, and are related to the physical inductance (L_1) and capacitance (C_1) of the full m-derived section by:

$$L = \frac{2m}{1 + m^2} L_1 \; ; \quad C = \frac{1}{2m} C_1 \tag{AII-2}$$

Substitution of (AII-2) into (AII-1) yields for time delay per section, interms of the physical components:

$$d = 2m\sqrt{\frac{L_1 C_1}{m^2 + 1}} \tag{AII-3}$$

$$d = 1.586\sqrt{L_1 C_1} \; ; \quad m = 1.3$$

The characteristic impedance of the filter section is defined as:

$$Z_o = \sqrt{\frac{L}{C}} \tag{AII-4}$$

Substitution of (AII-2) into (AII-4) yields:

$$Z_o = \frac{2m}{\sqrt{m^2+1}} \times \sqrt{\frac{L_1}{C_1}}$$

$$Z_o = 1.586\sqrt{\frac{L_1}{C_1}} \quad ; \quad m = 1.3 \qquad \text{(AII-5)}$$

Division of equations (AII-3) and (AII-5) yields:

$$C_1 = \frac{d}{Z_o} \qquad \text{(AII-6)}$$

Multiplication of equations (AII-3) and (AII-5) yields:

$$L_1 = 2.5dZ_o \qquad \text{(AII-7)}$$

Thus a solution for the requisite values of physical inductance and capacitance may be obtained from the specified characteristic impedance and a determination of the delay per section.

The delay per section is a function of the total delay (T) specified and of the number of sections (N) with which this is to be accomplished. Specifically, in a first analysis:

$$T = Nd$$

If, however, the customary interpretation of delay is to be obeserved: that this quantity be measured at the 50% point of the output response of the delay line when a step function input is applied, it becomes necessary to add to the right side of this equation a term equal to half the rise time (T_r) of the delay line. Thus:

$$T = Nd + \tfrac{1}{2}T_r \qquad \text{(AII-8)}$$

A straightforward Laplace transform analysis of a single full m-derived T section yields, for a step function input:

$$T_{r1} = \frac{1}{2.9F_c} , \qquad \text{(AII-9)}$$

where the section rise time (T_{r1}) is taken between the 10% and 90% points of the output and the cutoff frequency (F_c) is defined by:

$$F_c = \frac{1}{2\pi\sqrt{LC}}$$

In terms of the physical components L_1 and C_1, this becomes:

$$F_c = \frac{1}{2\pi}\sqrt{\frac{m^2+1}{L_1 C_1}} \qquad \text{(AII-10)}$$

$$F_c = \frac{0.261}{\sqrt{L_1 C_1}} \quad ; \quad m = 1.3$$

Substitution of (AII-10) into (AII-9) yields:

$$T_{r1} = 1.32\sqrt{L_1 C_1} \qquad \text{(AII-11)}$$

A comparison of equations (AII-3) and (AII-11) shows that:

$$d = \frac{1.586}{1.32} T_{r1} = 1.2\, T_{r1} \qquad \text{(AII-12)}$$

Substitution of equation (AII-12) into (AII-8) yields for total delay (T) in terms of the single and multi-section rise times T_{r1} and T_r respectively:

$$T = 1.2NT_{r1} + \tfrac{1}{2}T_r \qquad \text{(AII-13)}$$

Finally, substitution of the result of Appendix I (AI-1) into

equation (AII-13) yields as the fundamental equation describing the overall performance of a multi-section lumped parameter delay line:

$$T = \left[1.2N^{(2/3)} + \tfrac{1}{2}\right] T_r = XT_r \qquad \text{(AII-14)}$$

This expression permits the requisite number of sections to be determined in terms of two of the specifications which ordinarily are given for a pulse delay network.

Once the appropriate number of sections has been determined, equation (AII-14) may easily be manipulated to yield an expression from which the delay per section may be determined. This latter quantity is necessary in order to complete the detailed design (see equations AII-6 and AII-7). Substituting equation (AI-1) of Appendix I into (AII-8), we have:

$$T = Nd + \tfrac{1}{2}N^{(1/3)}T_{rl} \qquad \text{(AII-15)}$$

Substitution of (AII-12) into (AII-15) yields:

$$T = \left[N + \frac{1}{2.4}N^{(1/3)}\right]d = Yd \qquad \text{(AII-16)}$$

Thus, the equations upon which the design of a lumped parameter delay network rests are complete.

APPENDIX III

MULTILAYER COIL DESIGN

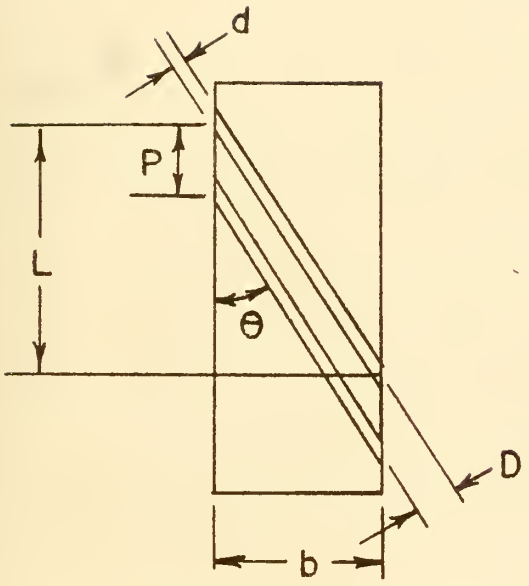


Figure 14

b: axial depth of coil
d: wire diameter
D: perpendicular separation of wires
L: segment length
M: turns per layer
N: crossovers per turn
P: linear progression
R: mean radius of 1st layer
R_i: mandrel radius
Θ: crossover angle
Ø: angular progression

(1) $R = R_i + d/2$

(2) $2\pi R/N = L$

(3) Using:

$$\theta = \tan^{-1}(b/L)$$

and: $D = b\cos(\theta)/M$

in: $P = D/\sin(\theta)$,

$$P = b\cos(\theta)/M \sin(\theta) = b\cot(\theta)/M = bL/Mb = L/M$$

(4) $180P/R\pi = \phi$

(5) $180N/(360 \pm \phi)$ = mandrel-cam gear ratio

EXAMPLE

The design of the 28.6 uh coils will be carried out:

$R = 0.125 + 0.0025 = 0.1275$ (R_1 was chosen = 1/8")

$L = 2\pi \times 0.1275/2 = 0.401$ (N was chosen = 2)

$P = 0.401/7.5 = 0.0535$ (M was found to be 7.5)

$\phi = 0.0535 \times 180/\pi \times 0.1275 = 24^{\circ}$

$180 \times 2/(360-24) = 360/336 = 90/84$

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